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(54) **Data transfer system**

(57) ATM data can be transferred via a highspeed serial data bus standardized by the IEEE 1394 format. In a data transferring apparatus for transferring data by employing a serial bus standardized by the IEEE 1394 format, an ATM cell transferring apparatus is comprised of an adding circuit for adding a predetermine header in order that an ATM cell used in a network defined by the ATM system is stored into the data field of the isochronous packet defined by the IEEE 1394 format.

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Description

The present invention generally relates to the transfer of data and in particular to: a data transfer method; a data transfer apparatus; a data receiving method; a data receiving apparatus; and a link-layer controlling circuit.

Embodiments of the present invention are directed to data communication techniques capable of transferring ATM (Asynchronous Transfer Mode) data via a serial data bus standardized by IEEE 1394.

Recently, communication systems have been proposed in which various electronic appliances such as personal computers, digital video cameras, digital tuners, and hard disk units are electrically connected to each other by employing a highspeed serial data bus standardized by IEEE 1394 (will be referred to as a "1394-serial data bus" hereinafter) so as to communicate digital picture/image signals, digital audio/voice signals, and the like among these electronic appliances. In the above-described data communication systems, since the respective electronic appliances are connected to each other via the cables defined in IEEE 1394 (will be referred to as "1394-cables" hereinafter), the digital image signals and the digital audio signals can be communicated among these electronic appliances. Furthermore, all of these electronic appliances can be controlled in total sense.

On the other hand, ATM (Asynchonous Transfer Mode) is used in networks, e.g., a personal computer LAN (Local Area Network) and a B-ISDN (Broadband Integrated Service Digital Network). It should be noted that this ATM corresponds to such a format defined by ITU-T (International Telecommunication Union-Telecommunication). A packet (normally, called as a "cell") used in an ATM system owns a fixed length of 53 bytes, as illustrated in Fig. IA, which is constructed of a 5-bite ATM cell header, and a 48-byte payload subsequent to this ATM cell header. Then, the 5-byte cell header owns such a structure as shown in Fig. 1B. Since no synchronous relationship is required between a phase of a frame and a position of a cell, and/or between positions of cells within an ATM network, this ATM system is suitably used to constitute networks where data having various bite rates are communicated in mixture manners. Under such circumstances, strong needs are made of establishing a networks with satisfying both the merits of the above-described communication system and ATM system.

The present invention provides data transferring method/apparatus capable of transferring an ATM cell via a 1394-serial data bus.

An ATM cell transferring method, according to an aspect of the present invention, is featured by that a data transferring method for transferring data by employing a serial bus standardized by the IEEE 1394 format, wherein: a predetermined header is added to an ATM cell used in a network defined by the ATM system in such a manner that the ATM cell is transferred by using the structure of the isochronous packet defined by the IEEE 1394 format.

Also, an ATM cell transferring apparatus, according to another aspect of the present invention, is featured that in a data transferring apparatus for transferring data by employing a serial bus standardized by the IEEE 1394 format, an ATM cell transferring apparatus is comprised of: an adding circuit for adding a predetermined header in order that an ATM cell used in a network defined by the ATM system is stored into the data field of the isochronous packet defined by the IEEE 1394 format.

In accordance with the present invention, the ATM cell can be entered into the isochronous packet defined by IEEE 1394, and then can be sent out to the 1394-serial data bus.

A more complete understanding of the present invention may be acquired by referring to the following illustrative description and the accompanying drawings, in which like reference numbers indicate like features and wherein:

Fig. 1A and Fig. 1B schematically illustrate a structure of an ATM cell used in an ATM system;

Fig. 2A to Fig. 2D illustratively show a process operation for transferring an ATM cell via the 1394-serial data bus in accordance with the present invention;

Fig. 3 schematically represents an example of a structure of an isochronous packet transferred via the 1394-serial data bus according to the present invention;

Fig. 4 illustratively indicates contents of the 1394-isochronous packet header to the cell header shown in Fig. 3;

Fig. 5 schematically shows another example of a structure of an isochronous packet transferred via the 1394-serial data bus according tot he present invention; and

Fig. 6 is a schematic block diagram for representing an arrangement of an ATM cell transferring apparatus, according to an embodiment of the present invention, capable of executing the process operation for transferring the ATM cell via the 1394-serial data bus.

Referring now to drawings, ATM cell transferring method/apparatus according to various preferred embodiments of the present invention will be described in detail.

First, Fig. 2 is an illustration used to explain a process operation for processing an ATM cell which will then be transferred via a 1394-serial data bus (namely, a serial data bus defined by IEEE 1394). This process operation will be explained more in detail with reference to Fig. 6.

As shown in Fig. 2A, a source packet header is add-

ed to a head portion of the inputted ATM source packet (namely, ATM cell of Fig. 1A) to thereby produce such an ATM source packet as represented in Fig. 2B. Subsequently, as represented in Fig. 2C, in response to timing at which the ATM source packet is reached to an Iso packet transmit/receive FIFO 13 (will be explained later), a CIP (Common Isochronous Packet) header is added to a head portion of a single (ATM cell + source packet header), or head portions of plural (ATM cells + source packet headers), depending upon conditions of transfer permissions to the 1394-cable. Next, as indicated in Fig. 2D, a 1394-isochronous packet header is added to the resulting ATM cell + source packet header, so that such an isochronous packet is obtained by storing the ATM cell into the data field of the isochronous packet. Then this resulting isochronous packet is sent out to the 1394 serial bus on the basis of timing of a cycle start packet flowing through the 1394 serial bus at a rate of 125 μ sec. It should be noted that these source packet header, CIP header, and 1394-isochronous packet header will be described more in detail.

Fig. 3 illustrates a structural example of the isochronous packet to be transferred via the 1394-serial data bus, as indicated in Fig. 2. Fig. 4 illustrates 7-byte contents of the isochronous packet from the header thereof to the cell header, shown in Fig. 3. It should also be noted that numerals in blanks of Fig. 4 indicate bite numbers. Also, it should be understood that this isochronous packet is transferred in such a way that a left end of the 1394-isochronous packet header positioned at an upper end is firstly transferred, and a right end of the data CRC positioned at a lower end is finally transferred. Referring now to Fig. 3 and Fig. 4, a description will be made of the isochronous packet.

The 1394-isochronous packet header has a length of 8 bytes, and is constituted by a data length (2 bytes) indicative of a length of data subsequent to this header; a tag (2 bits) for indicating as to whether or not the CIP header is present; a channel (6 bits) representative of a channel number through which the isochronous packet is transferred; a t-code (4 bits) indicative of a sort of a packet; an sy (4 bits) for indicating an order of the packet; and also a header CRC (4 bytes).

A 6-bit source node ID (SID) contained in the CIP header represents a node ID of an electronic appliance for sending out an isochronous packet with respect to the 1394-serial data bus. A 1-byte data block size (DBS) is a numeral for indicating a length of a data block in unit of a quadlet (= 4 bytes). A 2-bite fraction number (FN) indicates the number of data blocks where a source packet is subdivided. A 3-bit quadlet padding counter (QPC) is used when the FN owns a value except for "0". A 1-bit SPH is set to "1" in the case that a source packet owns a specific source packet header. As a result, this SPH is set to "1" in this case. A data block counter (DBC) is an 8-bit continuous counter, and is used so as to detect a dropout in a source packet transfer. A 6-bit format ID field (FMT) indicates a format of data to be transferred. In this case, the FMT of 0x28 indicates ATM data. A specification of a 3-byte format depend field (FDF) is determined by the FMT.

Subsequent to the CIP header, ATM data in unit of 15 quadlets (1 quadlet = 4 bytes) is transferred. The 15-quadlet data is arranged by a 1-quadlet source packet header, a 2-quadlet cell header, and a 12-quadlet payload.

A cycle count and a cycle offset of a source packet header correspond to time stamp information made by producing time instant information in unit of 125 μ sec based upon a transmission time instant of a packet. This time stamp information is given from a cycle master to this source packet header. The cycle offset is given to the counting operation every 40 ns, and the cycle count value is carried up every 125 μ sec. The cycle count value is sequentially counted up in such a manner that 1 count is made at 125 μ sec and a 2 counts are made at 250 μ sec. These cycle count and cycle offset are such values stored in a cycle time register provided within a preselected appliance, which is designated as the cycle master and is connected on the 1394-serial bus (see Fig. 6). The values are stored into the cycle time register based upon time instant information generated from a master clock generator.

This value is stored into the cycle start packet sent out to the 1394-serial data bus. As a consequence, this value is supplied to other appliances connected on the 1394-serial data bus. It should be noted that the structure of the source packet header is equivalent to such a structure defined by an MPEG type transport stream (MPEG-TS) (will be explained later).

The content of the cell header is shown in Fig. 1B. Since this content is well known in the art, no further explanation thereof is made in this specification. It should be understood that symbol "reserved" of 3 bytes is additionally provided as padding in front of the 5-byte ATM cell header in this embodiment mode, this cell header has such a structure that a head portion of the payload starts from a head portion of a quadlet. This padding process operation is carried out in an ATM signal process interface 12 shown in Fig. 6 (will be discussed later).

The data CRC corresponds to an error correction code for a data field (defined from CIP header up to finally transferred cell) of the isochronous packet.

As previously described, a merit of the structures indicated in Fig. 3 and Fig. 4 is achieved by that the ATM cell can be sent out on the 1394-serial data bus. Another merit is achieved by that the source packet header owns a similar structure to that of the transport stream of MPEG. As a consequence, since such circuit blocks (will be explained later) as the Iso packet transmit/receive FIFO 13, a header/sync information adding circuit 14, and a header removing/sync information recovering circuit 15 can be commonly used in the MPEG-TS signal system, a link layer control IC can be commonly used in the circuit arrangement of Fig. 6. Therefore, there are

advantages with respect to the design aspect and the manufacturing cost aspect. Moreover, it is possible to execute a time stamp process operation for absorbing a jitter phenomenon (will be explained later).

In the structures of Fig. 3 and Fig. 4, the 3-byte symbol "reserved" is entered in front of the ATM cell header. Alternatively, the 3-byte symbol "reserved" may be entered not in front of, but after the ATM cell header, so that a total length of the ATM source packet is equal to a length multiplied by 4 bytes × an integer (in this case, 56 bytes). In this alternative case, Fig. 5 represents a structure of an isochronous packet.

Now, a description will be made of an apparatus capable of executing the previously explained process operation for transferring the ATM cell via the 1394-serial data bus, for instance, a set top box (STB) connected to an ATM network. Fig. 6 schematically represents an internal arrangement of this set top box (STB), i.e., mainly shows a link layer control IC (will be referred to as a "LINK" hereinafter). This processing apparatus is equipped with a physical layer control IC (will be referred to as a "PHY" hereinafter), a LINK 2, a microprocessor 3, an ATM signal processing system 4, and a PLL 5.

The PHY 1 may initialize a bus, and may arbitrate a use right, and so on. Also, the PHY 1 may communicate data (data) such as an ATM cell, and various control signals (control) between the LINK 2 and this PHY 1, and further may transmit/receive these data and control signals to/from the 1394-data bus cable. Also, the PHY 1 may supply a system. clock (sysclk). The content of this LINK 2 will be described more in detail. The microprocessor 3 controls both the PHY 1 and the LINK 2, and acquires a range (band) of an isochronous communication. The ATM signal processing system 4 receives ATM data supplied from a terminal connected to an ATM network existing outside this step top box, and then produces/resolves an ATM cell. Otherwise, this ATM signal processing system 4 transmits such an ATM cell directly entered therein the ATM network to the ATM signal process interface 12. Also, this ATM signal processing system 4 supplies a basic frequency clock of 8 KHz owned by the ATM network to an 8 KHz-cycle control circuit 16. The PLL 5 reproduces a clock signal (clk) of an electronic appliance provided on the transmission end from timing information (above-described time stamp information) derived from a source packet header attached to an ATM cell received via the 1394-cable. This timing information is derived by the header removing/sync information recovering circuit 15 from the source packet header among the data received from the 1394-cable. It should be understood that when the timing information is not received via the 1394-cable, this PLL 5 may oscillate the clock signal in the self-oscillating manner. Then, this clock signal is supplied to the LINK 2 and the ATM signal processing system 4.

The internal arrangement of the LINK 2 may be mainly subdivided into an isochronous system, an asynchronous system, and a basic block. The isochronous system corresponds to such a block for producing an analyzing an isochronous packet on which data of an ATM cell is superimposed. The asynchronous system corresponds to such a block for producing and analyzing an asynchronous packet on which a control signal is superimposed. This control signal is, for instance, a command used to control an electronic appliance.

The asynchronous system is arranged by a microprocessor interface 6, a control register 7, an asynchronous packet transmission FIFO 8, an asynchronous packet reception FIFO 9, and a self-ID packet processing block 10.

The basic block 11 is equipped with a clock, a CRC, a physical layer interface a transmission block, a reception block, and the like.

The isochronous system is constituted by an ATM signal interface 12, an isochronous packet transmit/receive FIFO 13, a header/sync information adding circuit 14, a header removing/sync information recovering circuit 15, and an 8 KHz-cycle control circuit 16.

The microprocessor interface 6 may transmit/receive data in response to a demand issued from an upper grade layer between the microprocessor 3 and this microprocessor interface 6.

The data is written into a predetermined storage position of the control register 7 under control of the microprocessor 3, so that the operation of the LINK 2 is controlled. When the asynchronous packet is transmitted/received, a predetermined address of the control register 7 is read/written. Furthermore, a portion of the header of the isochronous packet is transmitted and received by utilizing this control register 7. For example, the above-described SID contained int he CIP header is supplied to the control register 7 from the basic block 11, and the control register 7 transfers the information of the source node ID via the microprocessor interface 6 to the microprocessor 3. As a result, the information about the original source node can be recognized by this set top box (STB) without being removed by the header removing/sync information receiving circuit 15.

The packet produced by the microprocessor 3 is temporarily stored into the asynchronous packet transmission FIFO 8. The temporarily stored packet is read by the basic block 11 as soon as the bus is brought into the empty state.

The packet acquired from the bus is written into the asynchronous packet reception FIFO 9 by the basic block 11. The microprocessor 3 executes the reading operation after confirming such a fact that this asynchronous packet reception FIFO 9 is not brought into the empty state.

The self-ID packet processing block 10 processes the node information received while the bus is initialized, and senses which node may manage the number of nodes connected to the bus, and also the isochronous channel of the bus.

The physical layer interface of the basic block 11 performs a parallel-to-serial conversion of transmission

data, and a serial-to-parallel conversion of reception data. The transmission block judges a condition of the bus so as to control the packet transmission. Then, the reception block determines a write destination, depending upon the sort of the received packet, namely the asynchronous packet, or the isochronous packet.

The ATM signal processing interface 12 executes the above-described padding process operation for the data of the ATM signal processing system 4 during the signal transmission to thereby convert this data into the data with the isochronous packet format. During the signal reception, the ATM signal processing interface 12 performs an inverse process operation, namely removes the padded byte from the padding-processed data.

The isochronous packet transmit/receive FIFO 13 corresponds to such a FIFO having a transmission function of an isochronous packet and also a reception function of an isochronous packet. As previously explained, during the signal transmission, the ATM cell (see Fig. 2A) received from the ATM network is written via the ATM signal processing system 4 and the ATM signal processing interface 12 into this isochronous packet transmit/receive FIFO 13. There is a cycle packet flowing in a cycle of 125 μ sec on the 1394-cable. In response to this timing, the ATM cell which has been waited in the FIFO 13 is sent out to the 1394-serial data bus by the basic block 11 at such a stage that the transmission permission is issued. In this case, since the header adding process operation is instantaneously performed in the header/sync information adding circuit 14, there is no problem with respect to the temporal aspect. As previously explained, since the ATM cell is waited in the FIFO 13, the ATM cell buffering operation is carried out, so that the jitter phenomenon of the ATM cell can be avoided. In general, a source of an ATM cell becomes unstable, because a jitter phenomenon on the order of 2 msec occurs. Therefore, a buffering operation by a FIFO may constitute a significant operation. Even when the source of the ATM cell sends out the cell under constant cell rate, the time interval between the ATM cells is greatly varied, since the cell sending time is delayed every time the ATM cell has passed several ATM switches. As a consequence, there is a certain possibility in delaying of such a cycle that a plurality of ATM cells are sent out in a continuous manner. Accordingly, the source packet header is added to each of the ATM cells (see Fig. 1B). Then, the CIP header and the 1394-isochronous packet header are properly added to such a cell which is outputted in connection with the cycle on the 1394-serial data bus (see Fig. 2C and Fig. 2D), and then the resulting cell is transferred to the 1394-serial data bus. In the case that an MPEG-TS type signal is transmitted/received, a communication is established between this isochronous packet transmit/receive FIFO 13 and an external appliance (not shown) via the MPEG-TS processing interface 17. In this case, a path is selected iv a switching unit 18. It should also be noted that the MPEG-TS signal is inputted via the 1394 cable, identification data contained in the header of this MPEG-TS signal is detected by the header removing/sync information recovering circuit 15, and the switching unit 18 is controlled in response to the detected identification data. In the case of the MPEG-TS system, since the source is relatively constant (jitter on the order of 200 μ sec), there is not so much jitter, as compared with that of the ATM cell. However, when the MPEG-TS type signal is transferred to the 1394-serial data bus in the cycle of 125 μ sec, and also is received therefrom, there is a temporal shift in the transmission system. As a consequence, this isochronous packet transmit/receive FIFO 13 may also play a role capable of absorbing this temporal shift. As previously described, the jitter problem can be improved by buffering the cell and by adjusting the cell rate before the cell is transferred to the 1394-serial data bus.

Also, since the peak rate of the cells appearing on the 1394-serial data bus can be lowered, the range used in the isochronous communication can be saved. After the isochronous packet which has been received from the 1394-serial data bus and acquired via the PHY 1 and the basic block 11 is converted into the structure of the ATM cell by the header removing/sync information recovering circuit 15, the resulting ATM cell packet is written into the isochronous packet transmit/receive FIFO 13 in such a range that the ATM cells are not overflown from this FIFO 13. The timing of the written ATM cell packet at which this ATM cell packet is outputted from the LINK 2 to the ATM signal processing system 4 is produced in response to the clock signal which is reproduced by the PLL 5 based upon the timing information contained in the header separated by the header removing/sync information recovering circuit 15.

The header/sync information adding circuit 14 adds the source packet header, the CIP header, and the 1394-isochronous packet header, as indicated in Fig. 3 and Fig. 4, to the cell read out from the isochronous packet transmit/receive FIFO 13. At this time, since the cycle count and the cycle offset within the source packet header are set with reference to the value of the clock employed in the basic block, the time stamp may be given to the cell. This clock is adjusted to the reference time based upon the time instant information contained in the cycle start packet sent from the cycle master, and also is counted up by the 8 KHz-cycle control circuit 16.

The header removing/sync information recovering circuit 15 removes the 1394-isochronous packet header, the CIP header, and the source packet header from the isochronous packet received from the basic block 11, and thereafter writes only the cell into the isochronous packet transmit/receive FIFO 13.

The 18 KHz-cycle control circuit 16 causes the signal having the frequency of 8 KHz owned by the ATM network to be synchronized with the signal having the frequency 'of 8 KHz (125 μ sec) appearing in the 1394-serial data bus. In other words, the timing of 8 KHz

derived from the ATM network is acquired via the ATM signal processing system 4, and also the 8 KHz-signal of the cycle start packet obtained via the basic block 11 is synchronized with this 8 KHz-timing, so that the ATM cell can be handled on the IEEE 1394 system.

While an illustrative ATM cell transferring apparatus according to the present invention has been described in detail, the ATM cell can be transferred via the 1394-serial data bus for the communication purpose.

Claims

1. A data transferring method for transferring data by employing a serial bus standardized by the IEEE 1394 format, wherein:
   a predetermined header is added to an ATM cell used in a network defined by the ATM system in such a manner that said ATM cell is transferred by using the structure of the isochronous packet defined by the IEEE 1394 format.

2. A data transferring method as claimed in claim 1 wherein:
   when said ATM cell is mapped to a source packet having a byte length longer than a byte length of said ATM cell, a difference byte between said byte length of the ATM cell and said byte length of the source packet is added as padding to one of a head portion of said ATM cell and a last portion thereof.

3. A data transferring method as claimed in claim 2 wherein:
   said ATM cell is arranged by a payload having a 48-byte length and an ATM cell header having a 5-byte length to be added to said ATM cell; and when said ATM cell is mapped to said source packet having a 56-byte length, a 3-byte difference is added to one of a head portion of said ATM cell header and a last portion of said payload as the padding to thereby an ATM source packet.

4. A data transferring method as claimed in claim 1 wherein:
   said predetermined header added to said ATM cell contains a source packet header; and a structure of said source packet header is similar to the structure of the transport stream defined by the MPEG system.

5. A data transferring method as claimed in claim 4 wherein:
   said source packet header has cycle count data and cycle offset data.

6. In a data transferring apparatus for transferring data by employing a serial bus standardized by the IEEE 1394 format,

   an ATM cell transferring apparatus comprising: an adding circuit for adding a predetermined. header in order that an ATM cell used in a network defined by the ATM system is stored into the data field of the isochronous packet defined by the IEEE 1394 format.

7. An ATM cell transferring apparatus as claimed in claim 6, further comprising:

   a buffer for buffering said ATM cell; wherein: said buffer improves a jitter component produced when said ATM cell is sent out to said IEEE 1394 serial bus.

8. An ATM cell transferring apparatus as claimed in claim 6, further comprising:
   means for synchronizing a signal having a frequency of 8 KHz owned by the ATM network with a signal having a frequency of 8 KHz used in the 1394-serial bus.

9. A data receiving method for receiving an ATM cell used in a network defined by the ATM system, which is transferred by employing a serial bus standardized by the IEEE 1394 format, wherein:
   a predetermined header is removed in order to obtain said ATM cell stored into the data field of the isochronous packet defined by the IEEE 1394 format.

10. A data receiving method as claimed in claim 9 wherein:
    in order to obtain an ATM cell mapped to a source packet having a byte length larger than a byte length of said ATM cell, a difference byte between said byte length of the source packet and said byte length of the ATM cell, which has been added to one of a head portion of said ATM cell and a last portion thereof, is removed.

11. A data receiving method as claimed in claim 10 wherein:
    an ATM cell arranged by a payload having a 48-byte length and an ATM cell header having a 5-byte length is obtained by removing a 3-byte difference added to one of a head portion of said ATM cell header and a last portion of said payload is removed from an ATM source packet mapped to said source packet having a 56-type length.

12. A data receiving method as claimed in claim 9 wherein:
    a predetermined header removed from said ATM source packet contains a source packet header; and a structure of said source packet header is

similar to the structure of the transport stream defined by the MPEG system.

13. A data receiving method as claimed in claim 12 wherein:

said source packet header has cycle count data and cycle offset data.

14. In a receiving apparatus for receiving an ATM cell used in a network defined by the ATM system, which is transferred by employing a serial bus standardized by the IEEE 1394 format,

a data receiving apparatus comprising:
a removing circuit for removing a predetermined header in order that an ATM cell used in a network defined by the ATM system is stored into the data field of the isochronous packet defined by the IEEE 1394 format.

15. A link layer controlling integrated circuit comprising:

a basic block communicated with a serial bus standardized by the IEEE 1394 format;
an interface communicated with a network defined by the ATM system;
a removing circuit for removing a predetermined header in order to obtain an ATM cell received via said serial bus and stored in a data field of an isochronous packet;
an adding circuit for adding a predetermined header in order to store an ATM cell received from said ATM type network into the data field of said isochronous packet; and
a buffer provided between said adding circuit, said removing circuit, and said interface, for adjusting a rate.

FIG. 1A

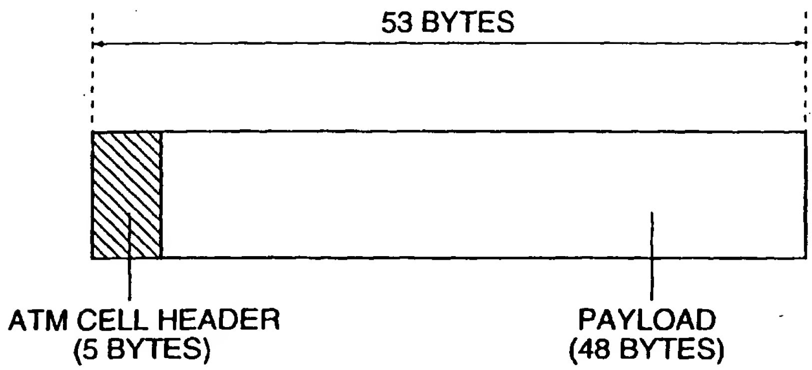
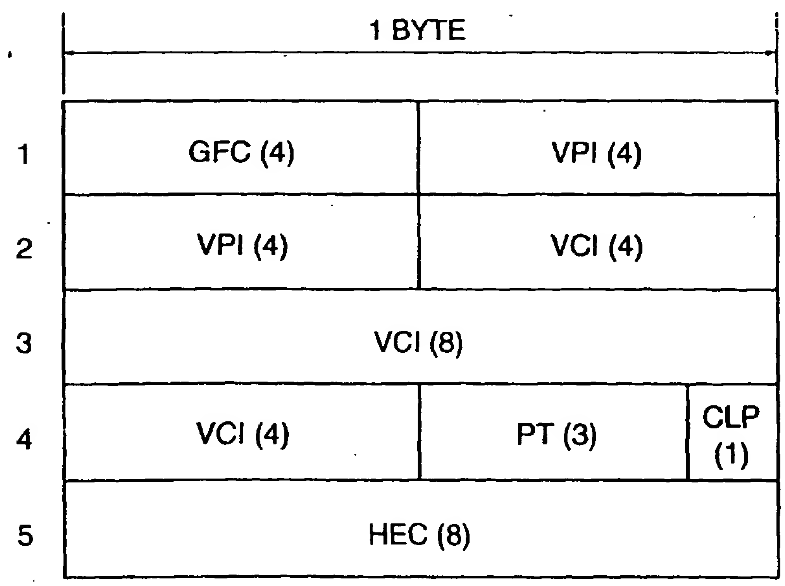


FIG. 1B



NUMERALS IN BLANKS
INDICATE BITE NUMBERS

FIG. 2A

FIG. 2B

FIG. 2C

FIG. 2D

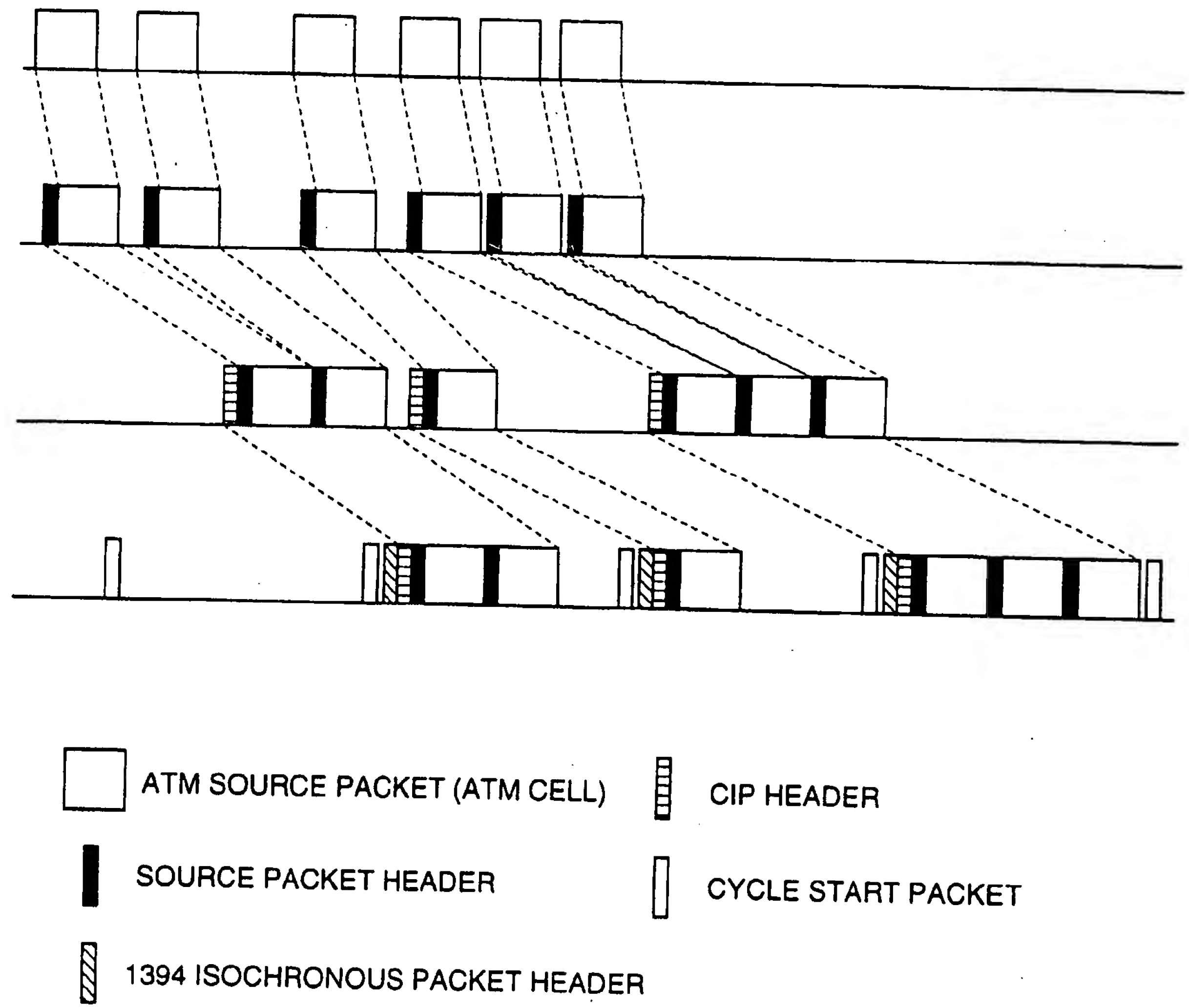


FIG.3

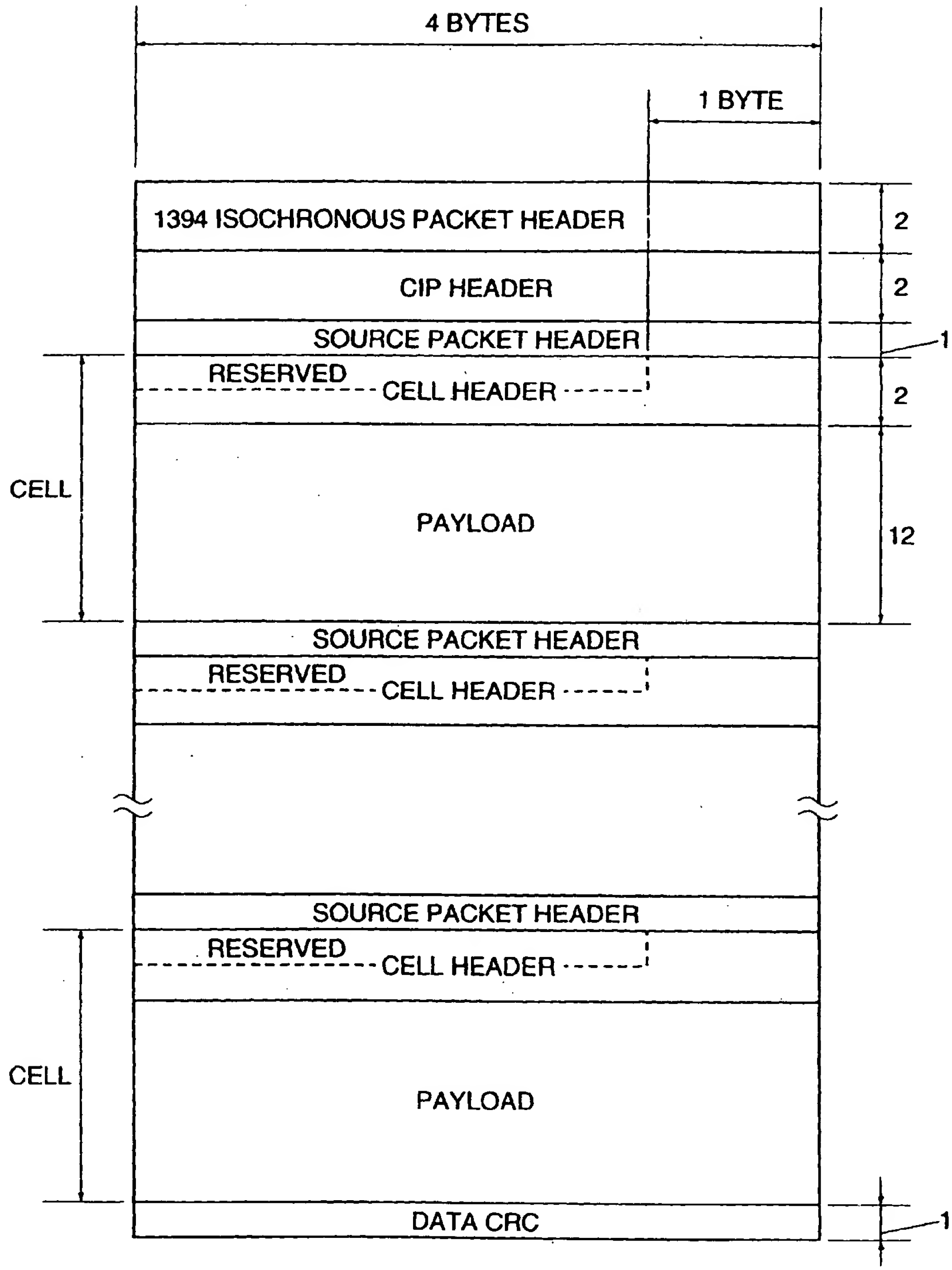
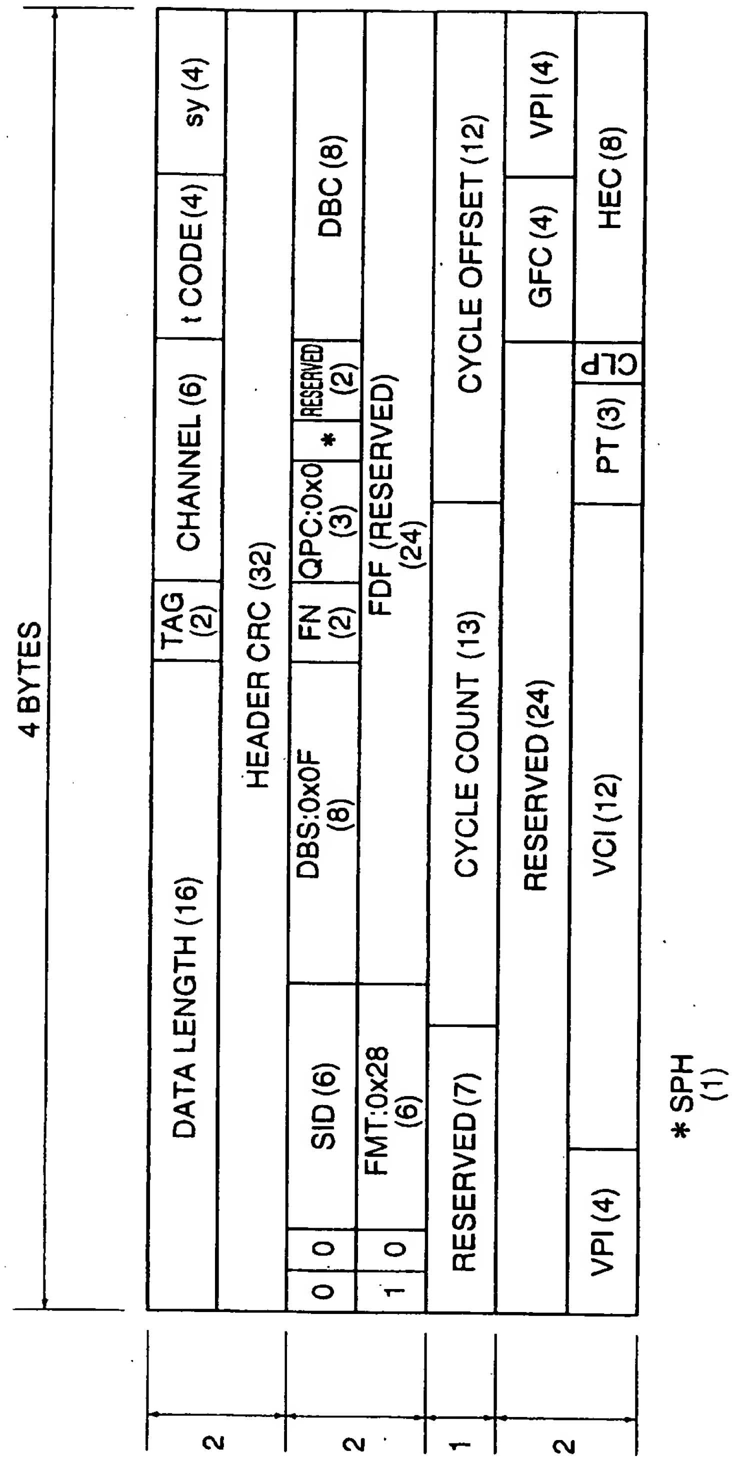

4 BYTES
1 BYTE
1394 ISOCHRONOUS PACKET HEADER
2
CIP HEADER
2
SOURCE PACKET HEADER
1
RESERVED
CELL HEADER
2
CELL
PAYLOAD
12
SOURCE PACKET HEADER
RESERVED
CELL HEADER
SOURCE PACKET HEADER
RESERVED
CELL HEADER
CELL
PAYLOAD
DATA CRC
1

FIG.4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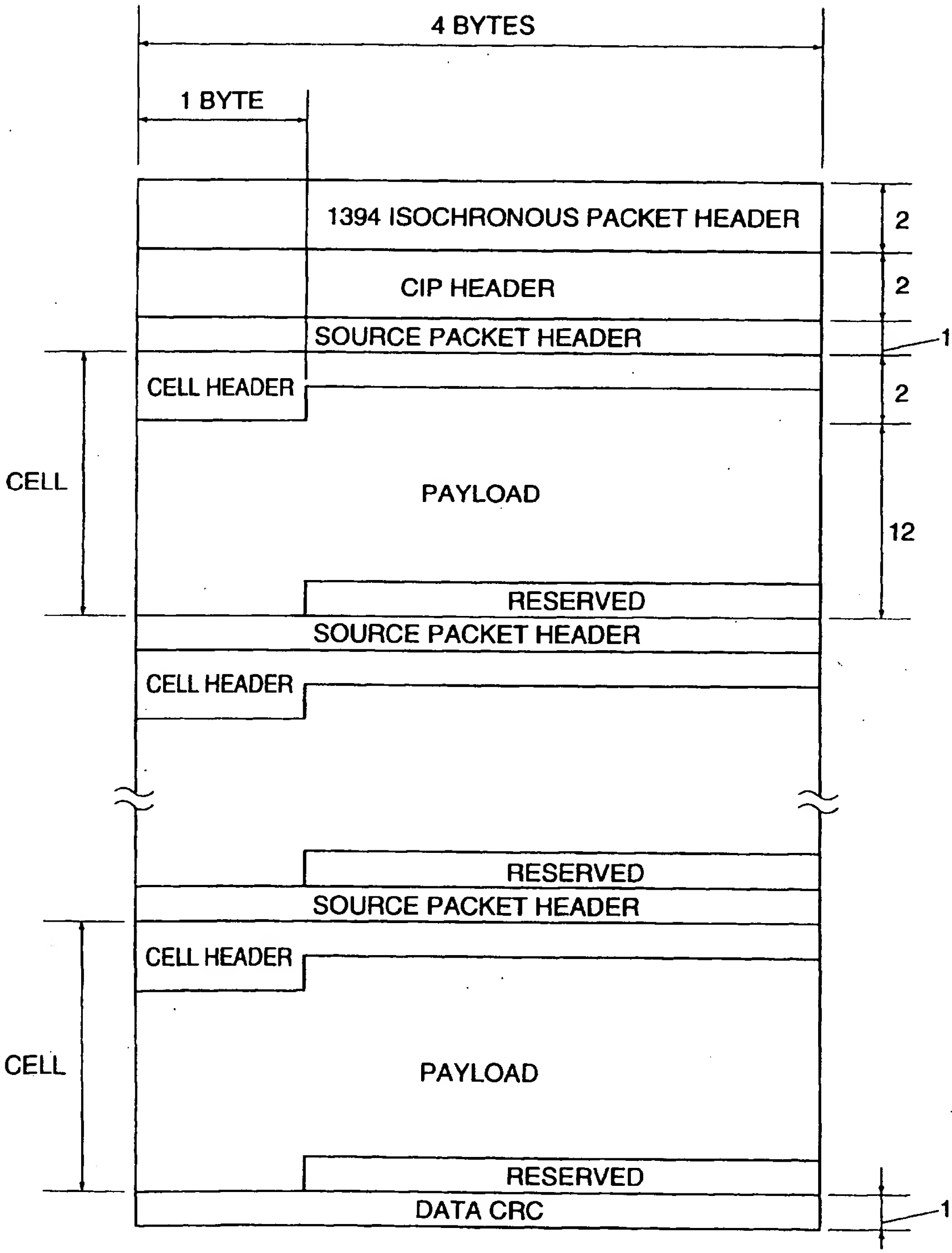
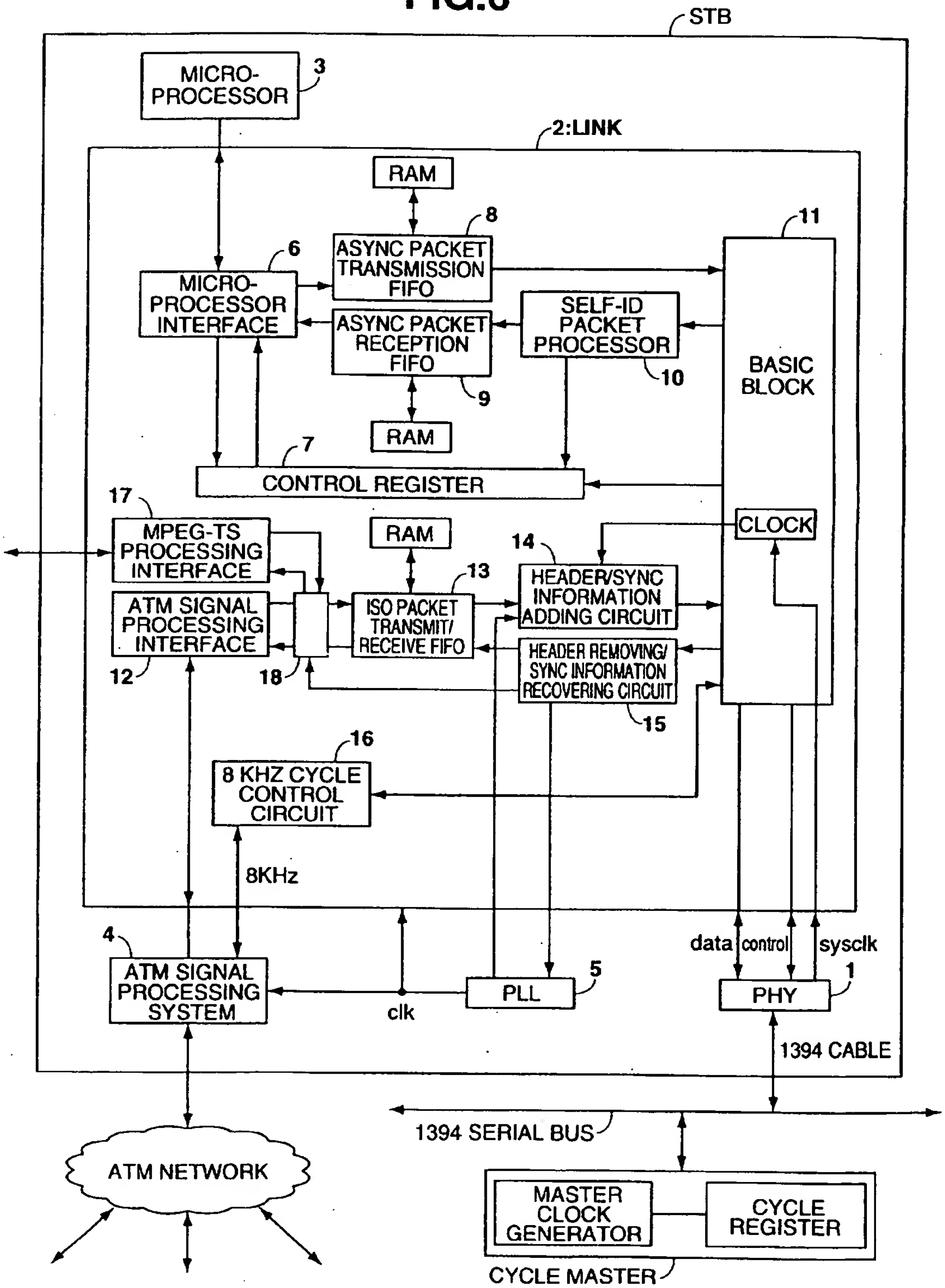
DATA LENGTH (16)
TAG (2)
CHANNEL (6)
t CODE (4)
sy (4)
HEADER CRC (32)
0 0
SID (6)
DBS:0x0F (8)
FN (2)
QPC:0x0 (3)
*
RESERVED (2)
DBC (8)
1 0
FMT:0x28 (6)
FDF (RESERVED) (24)
RESERVED (7)
CYCLE COUNT (13)
CYCLE OFFSET (12)
RESERVED (24)
GFC (4)
VPI (4)
VPI (4)
VCI (12)
PT (3)
CLP
HEC (8)
* SPH (1)
2
2
1
2

FIG.5



4 BYTES
1 BYTE
1394 ISOCHRONOUS PACKET HEADER
2
CIP HEADER
2
SOURCE PACKET HEADER
1
CELL HEADER
2
CELL
PAYLOAD
12
RESERVED
SOURCE PACKET HEADER
CELL HEADER
RESERVED
SOURCE PACKET HEADER
CELL HEADER
CELL
PAYLOAD
RESERVED
DATA CRC
1

FIG.6


STB
MICRO-PROCESSOR
3
2:LINK
RAM
8
11
6
ASYNC PACKET TRANSMISSION FIFO
MICRO-PROCESSOR INTERFACE
ASYNC PACKET RECEPTION FIFO
SELF-ID PACKET PROCESSOR
10
BASIC BLOCK
9
RAM
7
CONTROL REGISTER
17
MPEG-TS PROCESSING INTERFACE
RAM
CLOCK
14
13
HEADER/SYNC INFORMATION ADDING CIRCUIT
ATM SIGNAL PROCESSING INTERFACE
ISO PACKET TRANSMIT/ RECEIVE FIFO
HEADER REMOVING/ SYNC INFORMATION RECOVERING CIRCUIT
12
18
15
16
8 KHZ CYCLE CONTROL CIRCUIT
8KHz
4
data
control
sysclk
ATM SIGNAL PROCESSING SYSTEM
PLL
5
1
PHY
clk
1394 CABLE
1394 SERIAL BUS
ATM NETWORK
MASTER CLOCK GENERATOR
CYCLE REGISTER
CYCLE MASTER